IN THE CLAIMS

Please cancel claims 32, 33, 53, 58, and amend the claims as follows:

1. - 20. (Cancelled)

21. (Currently Amended) A method of fabricating a transistor in a semiconductor substrate, the method comprising:

forming a source region and a drain region in a semiconductor substrate, a channel region being between the source region and the drain region;

forming an insulating layer on the channel region;

forming a floating gate on the insulating layer, wherein the floating gate comprises a silicon carbide compound $Si_{1-x}C_x$; ~~and~~

selecting x to be between 0 and 1.0;

forming an intergate dielectric over the floating gate; and

forming a polysilicon control gate over the intergate dielectric.

22. (Cancelled)

23. (Previously Presented) The method of claim 21, wherein x is selected such that a barrier energy between the gate and the insulator is between 0 eV and 2.8 eV.

24. (Previously Presented) The method of claim 21, wherein x is selected at a predetermined value that is between 0.5 and 1.0.

25. (Cancelled)

26. (Previously Presented) The method of claim 21 wherein x is selected such that the transistor has a charge retention time of between 1 second and 106 years.

27. - 28. (Cancelled)

29. (Previously Presented) The method of claim 21, wherein forming a gate further comprises:

depositing the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer using low pressure chemical vapor deposition to form a layer of gate material; and

etching the gate material to a desired pattern using a reactive ion etch process.

30. (Previously Presented) The method of claim 29 wherein etching the gate material further comprises using plasma etching in combination with the reactive ion etch process.

31. (Previously Presented) The method of claim 29, further comprising conductively doping the silicon carbide compound $Si_{1-x}C_x$ while depositing the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer.

32. - 35. (Cancelled)

36. (Previously Presented) The method of claim 21 wherein forming an insulating layer comprises forming a layer of gate oxide or a layer of tunnel oxide on the channel region by dry thermal oxidation.

37. (Previously Presented) The method of claim 21 wherein forming a source region comprises forming a p-type source region and a p-type drain region in an n-type silicon substrate, a channel region being between the p-type source region and the p-type drain region.

38. (Previously Presented) The method of claim 21 wherein forming a source region comprises forming an n-type source region and an n-type drain region in a p-type silicon substrate, a channel region being between the n-type source region and the n-type drain region.

39. (Previously Presented) The method of claim 21 wherein forming a gate further comprises doping the gate by ion implantation.

40. (Previously Presented) The method of claim 21 wherein forming a gate further comprises depositing the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer by low pressure chemical vapor deposition, or by low pressure rapid thermal chemical vapor deposition, or by decomposition of hexamethyl disalene using ArF excimer laser irradiation, or by low temperature molecular beam epitaxy, or by reactive magnetron sputtering, or by DC plasma discharge, or by ion-beam assisted deposition, or by ion-beam synthesis, or by laser crystallization, or by laser reactive ablation deposition, or by epitaxial growth by vacuum anneal.

41. (Previously Presented) The method of claim 40 wherein depositing the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer further comprises depositing a film of a polycrystalline or microcrystalline doped silicon carbide compound $Si_{1-x}C_x$ on the insulating layer.

42. (Previously Presented) The method of claim 21, further comprising:

forming a well region in the semiconductor substrate;

forming field oxide on the semiconductor substrate to define an active region;

oxidizing the gate by plasma oxidation to form a layer of oxide on the gate; and

depositing oxide over the gate, the source region, and the drain region by chemical vapor deposition.

43. (Currently Amended) A method of fabricating a transistor comprising:

forming a source region and a drain region in a substrate that are separated by a channel region in the substrate;

forming an insulating layer on the substrate;

forming a layer of a silicon carbide compound $Si_{1-x}C_x$ on the insulating layer wherein x is between 0 and 1.0; ~~and~~

removing portions of the insulating layer and the layer of the silicon carbide compound $Si_{1-x}C_x$ to form a gate on the substrate;

forming an intergate dielectric on the gate; and

forming a polysilicon control gate over the intergate dielectric.

44. (Previously Presented) The method of claim 43 wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ further comprises depositing the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer by low pressure chemical vapor deposition, or by low pressure rapid thermal chemical vapor deposition, or by decomposition of hexamethyl disalene using ArF excimer laser irradiation, or by low temperature molecular beam epitaxy, or by reactive magnetron sputtering, or by DC plasma discharge, or by ion-beam assisted deposition, or by ion-beam synthesis, or by laser crystallization, or by laser reactive ablation deposition, or by epitaxial growth by vacuum anneal.

45. (Previously Presented) The method of claim 43, further comprising:

forming a well region in the substrate;

forming field oxide on the substrate to define an active region;

doping the silicon carbide compound $Si_{1-x}C_x$ while forming the layer of the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer; and

wherein forming an insulating layer comprises forming a layer of gate oxide or a layer of tunnel oxide on a silicon substrate by dry thermal oxidation;

wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ comprises depositing a film of a polycrystalline or microcrystalline doped silicon carbide compound $Si_{1-x}C_x$ on the insulating layer; and

wherein removing comprises:

patterning the layer of the silicon carbide compound $Si_{1-x}C_x$; and

etching the layer of the silicon carbide compound $Si_{1-x}C_x$ and the insulating layer to form a gate with plasma etching, or reactive ion etching, or a combination of plasma etching and reactive ion etching.

46. (Currently Amended) The method of claim 43 wherein:

forming a source region comprises forming a source region and a drain region in a silicon substrate that are separated by a channel region in the silicon substrate~~; and~~

~~further comprising:~~

~~oxidizing the gate by plasma oxidation to form a layer of oxide on the gate; and~~

~~depositing oxide over the gate, the source region, and the drain region by chemical vapor deposition~~.

47. (Currently Amended) The method of claim 43 wherein:

forming a source region comprises forming a source region and a drain region in a silicon substrate that are separated by a channel region in the silicon substrate; and

~~further comprising:~~

forming an intergate dielectric on the gate further comprises oxidizing the gate by plasma oxidation to form ~~an~~ the intergate dielectric ~~on the gate; and~~

~~forming a polysilicon control gate over the intergate dielectric~~.

48. (Previously Presented) The method of claim 43, further comprising doping the layer of the silicon carbide compound $Si_{1-x}C_x$ with a p-type implantation of a boron dopant.

49. (Previously Presented) The method of claim 43, further comprising doping the layer of the silicon carbide compound $Si_{1-x}C_x$ with an n-type ion implantation.

50. (Currently Amended) A method of fabricating a transistor comprising:

forming a source region and a drain region in a silicon substrate that are separated by a channel region in the silicon substrate;

forming an insulating layer on the silicon substrate;

forming a layer of a silicon carbide compound $Si_{1-x}C_x$ on the insulating layer wherein x is between 0 and 1.0;

doping the layer of the silicon carbide compound $Si_{1-x}C_x$ with a p-type implantation; ~~and~~

removing portions of the insulating layer and the layer of the silicon carbide compound $Si_{1-x}C_x$ to form a gate on the silicon substrate;

forming an intergate dielectric on the gate; and

forming a polysilicon control gate over the intergate dielectric.

51. (Previously Presented) The method of claim 50 wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ further comprises depositing the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer by low pressure chemical vapor deposition, or by low pressure rapid thermal chemical vapor deposition, or by decomposition of hexamethyl disalene using ArF excimer laser irradiation, or by low temperature molecular beam epitaxy, or by reactive magnetron sputtering, or by DC plasma discharge, or by ion-beam assisted deposition, or by ion-beam synthesis, or by laser crystallization, or by laser reactive ablation deposition, or by epitaxial growth by vacuum anneal.

52. (Previously Presented) The method of claim 50, further comprising:

forming a well region in the silicon substrate;

forming field oxide on the silicon substrate to define an active region;

doping the silicon carbide compound $Si_{1-x}C_x$ while forming the layer of the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer; and

wherein forming an insulating layer comprises forming a layer of gate oxide or a layer of tunnel oxide on a silicon substrate by dry thermal oxidation;

doping the layer comprises doping the layer of the silicon carbide compound $Si_{1-x}C_x$ with a p-type implantation of a boron dopant;

wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ comprises depositing a film of a polycrystalline or microcrystalline doped silicon carbide compound $Si_{1-x}C_x$ on the insulating layer; and

wherein removing comprises:

patterning the layer of the silicon carbide compound $Si_{1-x}C_x$; and

etching the layer of the silicon carbide compound $Si_{1-x}C_x$ and the insulating layer to form a gate with plasma etching, or reactive ion etching, or a combination of plasma etching and reactive ion etching.

53. (Cancelled)

54. (Currently Amended) The method of claim 50 ~~, further comprising~~ wherein:

forming an intergate dielectric further comprises oxidizing the gate by plasma oxidation to form ~~an~~ the intergate dielectric ~~on the gate; and~~

~~forming a polysilicon control gate over the intergate dielectric~~.

55. (Currently Amended) A method of fabricating a transistor comprising:

forming a source region and a drain region in a silicon substrate that are separated by a channel region in the silicon substrate;

forming an insulating layer on the silicon substrate;

forming a layer of a silicon carbide compound $Si_{1-x}C_x$ on the insulating layer wherein x is between 0 and 1.0;

doping the layer of the silicon carbide compound $Si_{1-x}C_x$ with an n-type ion implantation; ~~and~~

removing portions of the insulating layer and the layer of the silicon carbide compound $Si_{1-x}C_x$ to form a gate on the silicon substrate;

forming an intergate dielectric on the gate; and

forming a polysilicon control gate over the intergate dielectric.

56. (Previously Presented) The method of claim 55 wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ further comprises depositing the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer by low pressure chemical vapor deposition, or by low pressure rapid thermal chemical vapor deposition, or by decomposition of hexamethyl disalene using ArF excimer laser irradiation, or by low temperature molecular beam epitaxy, or by reactive magnetron sputtering, or by DC plasma discharge, or by ion-beam assisted deposition, or by ion-beam synthesis, or by

laser crystallization, or by laser reactive ablation deposition, or by epitaxial growth by vacuum anneal.

57. (Previously Presented) The method of claim 55, further comprising:

forming a well region in the silicon substrate;

forming field oxide on the silicon substrate to define an active region;

doping the silicon carbide compound $Si_{1-x}C_x$ while forming the layer of the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer; and

wherein forming an insulating layer comprises forming a layer of gate oxide or a layer of tunnel oxide on a silicon substrate by dry thermal oxidation;

wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ comprises depositing a film of a polycrystalline or microcrystalline doped silicon carbide compound $Si_{1-x}C_x$ on the insulating layer; and

wherein removing comprises:

patterning the layer of the silicon carbide compound $Si_{1-x}C_x$; and

etching the layer of the silicon carbide compound $Si_{1-x}C_x$ and the insulating layer to form a gate with plasma etching, or reactive ion etching, or a combination of plasma etching and reactive ion etching.

58. (Canceled)

59. (Currently Amended) The method of claim 55 ~~, further comprising~~ wherein:

forming an intergate dielectric further comprises oxidizing the gate by plasma oxidation to form ~~an~~ the intergate dielectric ~~on the gate; and~~

~~forming a polysilicon control gate over the intergate dielectric~~.

60. (Currently Amended) A method of fabricating a floating gate transistor comprising:

forming a source region and a drain region in a substrate that are separated by a channel region in the substrate;

forming an insulating layer on the substrate;

forming a layer of a silicon carbide compound $Si_{1-x}C_x$ on the insulating layer wherein x is between 0 and 1.0;

removing portions of the insulating layer and the layer of the silicon carbide compound $Si_{1-x}C_x$ to form a floating gate on the substrate;

forming an intergate dielectric on the floating gate; and

forming a polysilicon control gate over the intergate dielectric.

61. (Previously Presented) The method of claim 60 wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ further comprises depositing the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer by low pressure chemical vapor deposition, or by low pressure rapid thermal chemical vapor deposition, or by decomposition of hexamethyl disalene using ArF excimer laser irradiation, or by low temperature molecular beam epitaxy, or by reactive magnetron sputtering, or by DC plasma discharge, or by ion-beam assisted deposition, or by ion-beam synthesis, or by laser crystallization, or by laser reactive ablation deposition, or by epitaxial growth by vacuum anneal.

62. (Currently Amended) The method of claim 60, further comprising:

forming a well region in the substrate;

forming field oxide on the substrate to define an active region;

doping the silicon carbide compound $Si_{1-x}C_x$ while forming the layer of the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer; and

wherein forming a source region comprises forming a source region and a drain region in a silicon substrate that are separated by a channel region in the substrate;

wherein forming an insulating layer comprises forming a layer of tunnel oxide on the silicon substrate by dry thermal oxidation;

wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ comprises depositing a film of a polycrystalline or microcrystalline doped silicon carbide compound $Si_{1-x}C_x$ on the insulating layer;

wherein removing comprises:

patterning the layer of the silicon carbide compound $Si_{1-x}C_x$; and

etching the layer of the silicon carbide compound $Si_{1-x}C_x$ and the insulating layer to form a floating gate with plasma etching, or reactive ion etching, or a combination of plasma etching and reactive ion etching; and

wherein forming an intergate dielectric comprises oxidizing the floating gate by plasma oxidation to form an intergate dielectric on the floating gate~~; and~~

~~wherein forming a control gate comprises forming a polysilicon control gate over the intergate dielectric~~.

63. (Previously Presented) The method of claim 60, further comprising doping the layer of the silicon carbide compound $Si_{1-x}C_x$ with a p-type implantation of a boron dopant.

64. (Previously Presented) The method of claim 60, further comprising doping the layer of the silicon carbide compound $Si_{1-x}C_x$ with an n-type ion implantation.

65. (Currently Amended) A method of fabricating a floating gate transistor comprising:

forming a source region and a drain region in a silicon substrate that are separated by a channel region in the silicon substrate;

forming an insulating layer on the silicon substrate;

forming a layer of a silicon carbide compound $Si_{1-x}C_x$ on the insulating layer wherein x is between 0 and 1.0;

doping the layer of the silicon carbide compound $Si_{1-x}C_x$ with an n-type ion implantation;

removing portions of the insulating layer and the layer of the silicon carbide compound $Si_{1-x}C_x$ to form a floating gate on the silicon substrate;

forming an intergate dielectric on the floating gate; and

forming a polysilicon control gate over the intergate dielectric.

66. (Previously Presented) The method of claim 65 wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ further comprises depositing the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer by low pressure chemical vapor deposition, or by low pressure rapid thermal chemical vapor deposition, or by decomposition of hexamethyl disalene using ArF excimer laser

irradiation, or by low temperature molecular beam epitaxy, or by reactive magnetron sputtering, or by DC plasma discharge, or by ion-beam assisted deposition, or by ion-beam synthesis, or by laser crystallization, or by laser reactive ablation deposition, or by epitaxial growth by vacuum anneal.

67. (Currently Amended) The method of claim 65, further comprising:

forming a well region in the silicon substrate;

forming field oxide on the silicon substrate to define an active region;

doping the silicon carbide compound $Si_{1-x}C_x$ while forming the layer of the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer; and

wherein forming an insulating layer comprises forming a layer of tunnel oxide on the silicon substrate by dry thermal oxidation;

wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ comprises depositing a film of a polycrystalline or microcrystalline doped silicon carbide compound $Si_{1-x}C_x$ on the insulating layer;

wherein removing comprises:

patterning the layer of the silicon carbide compound $Si_{1-x}C_x$; and

etching the layer of the silicon carbide compound $Si_{1-x}C_x$ and the insulating layer to form a floating gate with plasma etching, or reactive ion etching, or a combination of plasma etching and reactive ion etching; and

wherein forming an intergate dielectric comprises oxidizing the floating gate by plasma oxidation to form an intergate dielectric on the floating gate~~; and~~

~~wherein forming a control gate comprises forming a polysilicon control gate over the intergate dielectric~~.

68. (Currently Amended) A method of fabricating a memory cell comprising:

forming a source region and a drain region in a substrate that are separated by a channel region in the substrate;

forming an insulating layer on the substrate;

forming a layer of a silicon carbide compound $Si_{1-x}C_x$ on the insulating layer wherein x is between 0 and 1.0;

removing portions of the insulating layer and the layer of the silicon carbide compound $Si_{1-x}C_x$ to form a floating gate on the substrate;

forming an intergate dielectric on the floating gate; and

forming a polysilicon control gate over the intergate dielectric that is coupled to receive a control voltage from a memory device.

69. (Previously Presented) The method of claim 68 wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ further comprises depositing the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer by low pressure chemical vapor deposition, or by low pressure rapid thermal chemical vapor deposition, or by decomposition of hexamethyl disalene using ArF excimer laser irradiation, or by low temperature molecular beam epitaxy, or by reactive magnetron sputtering, or by DC plasma discharge, or by ion-beam assisted deposition, or by ion-beam synthesis, or by laser crystallization, or by laser reactive ablation deposition, or by epitaxial growth by vacuum anneal.

70. (Currently Amended) The method of claim 68, further comprising:

forming a well region in the substrate;

forming field oxide on the substrate to define an active region;

doping the silicon carbide compound $Si_{1-x}C_x$ while forming the layer of the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer; and

wherein forming a source region comprises forming a source region and a drain region in a silicon substrate that are separated by a channel region in the silicon substrate;

wherein forming an insulating layer comprises forming a layer of tunnel oxide on the silicon substrate by dry thermal oxidation;

wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ comprises depositing a film of a polycrystalline or microcrystalline doped silicon carbide compound $Si_{1-x}C_x$ on the insulating layer;

wherein removing comprises:

patterning the layer of the silicon carbide compound $Si_{1-x}C_x$; and

etching the layer of the silicon carbide compound $Si_{1-x}C_x$ and the insulating layer to form a floating gate with plasma etching, or reactive ion etching, or a combination of plasma etching and reactive ion etching;

wherein forming an intergate dielectric comprises oxidizing the floating gate by plasma oxidation to form an intergate dielectric on the floating gate; and

wherein forming a polysilicon control gate comprises forming a polysilicon control gate over the intergate dielectric that is coupled to receive a programming voltage or a read voltage from a memory device.

71. (Previously Presented) The method of claim 68, further comprising doping the layer of the silicon carbide compound $Si_{1-x}C_x$ with a p-type implantation of a boron dopant.

72. (Previously Presented) The method of claim 68, further comprising doping the layer of the silicon carbide compound $Si_{1-x}C_x$ with an n-type ion implantation.

73. (Currently Amended)A method of fabricating a memory cell comprising:

forming a source region and a drain region in a silicon substrate that are separated by a channel region in the silicon substrate;

forming an insulating layer on the silicon substrate;

forming a layer of a silicon carbide compound $Si_{1-x}C_x$ on the insulating layer wherein x is between 0 and 1.0;

doping the layer of the silicon carbide compound $Si_{1-x}C_x$ with an n-type ion implantation;

removing portions of the insulating layer and the layer of the silicon carbide compound $Si_{1-x}C_x$ to form a floating gate on the silicon substrate;

forming an intergate dielectric on the floating gate; and

forming a polysilicon control gate over the intergate dielectric that is coupled to receive a control voltage from a memory device.

74. (Previously Presented) The method of claim 73 wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ further comprises depositing the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer by low pressure chemical vapor deposition, or by low pressure rapid thermal chemical vapor deposition, or by decomposition of hexamethyl disalene using ArF excimer laser irradiation, or by low temperature molecular beam epitaxy, or by reactive magnetron sputtering, or by DC plasma discharge, or by ion-beam assisted deposition, or by ion-beam synthesis, or by laser crystallization, or by laser reactive ablation deposition, or by epitaxial growth by vacuum anneal.

75. (Currently Amended) The method of claim 73, further comprising:

forming a well region in the silicon substrate;

forming field oxide on the silicon substrate to define an active region;

doping the silicon carbide compound $Si_{1-x}C_x$ while forming the layer of the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer; and

wherein forming an insulating layer comprises forming a layer of tunnel oxide on the silicon substrate by dry thermal oxidation;

wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ comprises depositing a film of a polycrystalline or microcrystalline doped silicon carbide compound $Si_{1-x}C_x$ on the insulating layer;

wherein removing comprises:

patterning the layer of the silicon carbide compound $Si_{1-x}C_x$; and

etching the layer of the silicon carbide compound $Si_{1-x}C_x$ and the insulating layer to form a floating gate with plasma etching, or reactive ion etching, or a combination of plasma etching and reactive ion etching;

wherein forming an intergate dielectric comprises oxidizing the floating gate by plasma oxidation to form an intergate dielectric on the floating gate; and

wherein forming a <u>polysilicon</u> control gate comprises forming a polysilicon control gate over the intergate dielectric that is coupled to receive a programming voltage or a read voltage from a memory device.